REMARKS

These remarks are in response to the final Office Action mailed on February 4, 2003, and for which a two-month extension is requested. The Office Action rejected claims all of the pending claims under 35 U.S.C. 103(a) and claims 78, 79, and 81-85 under 35 U.S.C. 112. Claims 78, 81-83, and 85 have been amended for reasons related to the rejections under 35 U.S.C. 112, claims 15-25 and 75-77 have been cancelled, and several new claims have been added. Consequently, the present Amendment is being filed with a Request for Continued Examination. For the reasons described below, all of the currently pending claims are believed allowable. Claims 81-85 and the newly added claims are drawn to a particular aspect of the present invention, namely the modularity of the capacitor formation process, and are discussed first, followed by a discussion of the other pending claims, which are drawn embodiments for executing the various aspects of the present application.

<u>Modularity Aspect</u>

A major aspect of the present invention is the capability to selectively include a process for forming high quality capacitors into a transistor process flow incorporating an anti-reflective layer without having to alter the parameter values defining the transistor formation process. Claims 81-85, as well as the newly added claims, are drawn to this modularity aspect of the present invention. The Office Action rejected claims 81-85, stating that "As far as the examiner can ascertain, [the cited references] teach the limitations of claims 81-83 and 85 similar to claims 3, 8-11, 36, and 39 above." This is respectfully submitted to be in error, both in terms of the validity of the rejection as well as the ascertaining that these claims represent the same aspects and limitations of the present invention. Claims 3, 8-11, 36, and 39 are all drawn to a specific embodiment for the formation of an integrated circuit. Although the limitations and concepts of claims 81-85 can be implemented using this specific embodiment, claims 81-85, along with the newly added claims, are all drawn to a different aspect of the present invention that differs conceptually from these other claims, with corresponding differences appearing in the limitations of claims 81-85 and the newly added claims.

This aspect of the invention optimizes the transistor formation process flow, including the anti-reflective layer, while maintaining the modularity of the capacitor formation module. After optimizing the transistor flow (without the capacitor module), or using an existing transistor flow, the flow of the capacitor module is then optimized *while maintaining* the process defined for the transistor flow. This allows the capacitor module, whose step are executed in between steps of the transistor flow (see, for example, page 12, line 26, to page 13, line15), to be included or not as desired without having to reformulate the parameters defining the transistor flow. The formulation of the parameters defining such an optimized flow is quite involved and expensive. As described in the application, a principle aspect of the present invention is that parameter set defining the transistor process flow need not be changed dependent upon whether the circuit being formed includes capacitor.

This aspect is described beginning in the first sentence of the Description of Preferred Embodiment section, starting at page 8, line 15:

> **<u>Description of the Preferred Embodiment</u>**
> A primary objective of the present invention is to present a process for the integration of a high performance capacitor into a standard CMOS fabrication process flow. ... It is preferred that the steps required to form these capacitors should not require any change in the process parameters for the non-capacitor stages. ...

The importance of this aspect is also stressed at the end of the Description of Preferred Embodiment section. For instance, the lack of this advantage for an embodiment lacking this modularity is described beginning at line of page 15:

> However, as discussed above, this option would not allow the capacitor formation subprocess to be integrated into the fabrication process without a modification of process parameters and the consequent reformulation difficulties, as well as adding variation to the manufacturing steps required. The capacitor process module of steps 4-10 could no longer be included or excluded as needed without also altering the other portions of the process, particularly steps 11, 12, and 13 which immediately follow. ...

The difficulties resulting from the lack of this modularity aspect are also discussed on page 11, lines 15-30:

> However, this would not allow the capacitor formation subprocess to be integrated into the fabrication process without a modification of process parameters and the consequent reformulation difficulties, as well as adding variation to the manufacturing steps required. ... Such reparameterizations

> result in other process difficulties that would require resolution and necessitate two different process recipes, one for capacitors and one without capacitors.

The modularity aspect of the present invention, to which claims 81-85 and the newly added claims are drawn, overcome these process difficulties and require only a single process recipe for the transistor flow, independent of whether the capacitor module is included.

Consequently, the present invention provides a capacitor module that can be incorporated into the transistor flow without changing the parameters defining the transistor flow, but will still providing a high quality capacitor in the presence of the anti-reflective layer. Specific embodiments achieve this by the inclusion in the capacitor module, in addition to the top capacitor electrode and the inter-electrode dielectric, of an insulating structure optimized to electrically isolate the capacitor plates from one another. For instance, in the first exemplary embodiment, a thin conformal insulating layer is formed, prior to forming the anti-reflective layer, over the capacitor structure. As described in the application at page 12, lines 12-14, the process parameters for the insulating structure are selected so that the electrical insulation of the capacitor plates are optimized while maintaining the previously optimized transistor flow:

> The chosen thickness for the RTO layer is a compromise: It needs to be thick enough to fill in the undercut 180, yet thin enough to not significantly degrade a photolithographic process, particularly in the transistor sector, based on previously determined parameters.

Again, it should be noted that when the process flow, including the capacitor module, is executed, the capacitor specific steps occur in the middle of the transistor formation steps, whereas the process parameters defining the capacitor module are optimized while maintaining the previously optimized transistor flow. The parameters defining these steps for both the transistor flow and the capacitor module are optimized before they are used in an actual manufacturing process. During manufacture, the processing is then conducted according to these recipes.

New claims 86-90 are drawn to this formulation of the processing flows. In step a) of independent claim 86, the parameters for the process are defined: sub-step i) optimizes the parameters for the formation of transistor gates using an antireflective layer and sub-step ii) optimizes a capacitor module to electrically isolate the top electrode from the bottom electrode without changing the previously optimized parameter values of said

transistor flow. Step b) then forms an integrated circuit according to the process defined in step a).

New claims 91-96 are also drawn to this aspect and describe the use of these processes when capacitors are formed along with transistors in the same fabrication process, with the relation of the parameters defining the processes as a limitation. The claims describe the shared portions of the fabrication process (the first and second sectors of claim 91 respectively corresponding to the transistor and capacitor sectors of Figures 2-9) as "optimized for … gate formation" in the transistor sector. The additional steps, including the "forming an insulating structure over the capacitor structure", of the capacitor module that are performed in the second sector are then "performed according to a … set of process parameters optimized to electrically isolate [the] top electrode from the conductive layer while keeping [the] first set process parameters [for the shared steps the that have been optimized for gate formation] the same."

New claims 97-101 highlight the modularity aspect of the present invention, which allows the use of an anti-reflecting layer, while still maintaining the same set of process parameters for the transistor formation flow whether the capacitor module is included or not. The claims describe two processes, where the first flow is without the capacitor module and the second flow includes the capacitor module. The shared steps ("forming a conducting layer, forming a antireflective layer, forming a patterned photoresist layer, and etching the conductive layer") are the same in both cases, being "optimized for said gate formation", with the capacitor formation steps are "optimized for electrically isolating the top electrode from the second conductive layer while keeping first set of process parameters the same."

Returning to claims 81-85, these were rejected by the Office Action under 35 U.S.C. 103(a) since "As far as the examiner can ascertain, [the cited references] teach the limitations of claims 81-83 and 85 similar to claims 3, 8-11, 36, and 39 above." This is respectfully submitted to be incorrect, as claims 81-85 are drawn to the same aspect of the present invention as the newly added claims and recited specific limitations concerning these aspects, aspects that are not found in claims 3, 8-11, 36, and 39. More specifically, claim 81 (as amended) recites the limitation:

> wherein the process parameters of the portions of said process flow for forming one or more transistors prior to and subsequent to said performing a capacitor process module are optimized with the capacitor

process module omitted, and wherein the process parameters for the capacitor module are optimized for capacitor formation while maintaining the process parameters of said process flow for forming one or more transistors optimized with the capacitor process module omitted.

Claims 3-11, 36-39, and 72-74 are all drawn to specific embodiment in which this aspect of the invention can be executed, but do not in themselves contain this limitation. (Conversely, independent claim 81 is not specifically drawn to this embodiment, which is the subject of dependent claim 82.)

Claims 81-85 were also rejected under 35 U.S.C. 112, first paragraph. This rejection is also respectfully submitted to be without foundation. As the various extracts from the application quoted above show, the Applicants believe that this aspect of the invention is more than sufficiently described in the application. It is respectfully submitted that the comments of the Office Action with respect to this rejection are mixing up the order in which the various parameters defining the process are determined with the order in which the steps processes are executed. As discussed above, when a process defined by the parameter sets of the present is executed, the capacitor module occurs at an intermediate point between steps of the transistor flow (specifically, after forming the conductive layer, but prior to forming the anti-reflective layer); however, the parameter sets defining these process flows have been previously established. It is the relation of these parameter sets that is the subject of the quoted last element of claim 81.

Claim 81 was also rejected under 35 U.S.C. 112, second paragraph. Although this rejection is also believed to be in error, claim 81 has been rephrased to make its presentation clearer. In particular, the use of the language of "an optional capacitor module" has been remover. This phrase was used to highlight the modularity aspect of the present invention where the capacitor module can be included or not, as desired. The phrase is not believed to have been indefinite, however, as it was for "performing an optional capacitor module", not for "optionally performing a capacitor module", which is arguably indefinite. As the claim is drawn to the case where the capacitor module *is* included, the "optional" has been deleted and other portions of the claim language have been rationalized.

Claim 82, which is drawn to the case where the aspect of the invention found in claim 81 is executed according to the first embodiment, was also rejected under 35 U.S.C. 112, second paragraph. Claim 82 has been amended in response to the comments of the

Office Action and claims 82, 83, and 85 have also been amended to conform with the changes in their base claim, claim 81.

Particular Process Embodiments

Claims 3-11, 36-39, and 72-74 are drawn to a first exemplary embodiment of the formation of a capacitor in a CMOS process flow including an anti-reflective layer. These claims are believed allowable over the prior art for a number of reasons, as described in previous Amendments. Specifically, neither the occurrence of this inter-plate undercutting (180, Figure 3) nor the subsequent introduction of a conformal dielectric layer into this inter-plate region is found in the prior art, a limitation found in independent claims 3, 4, and 36. For example, claim 3 contains the language:

> ...subsequently removing at least a portion of said exposed portion of the dielectric layer to expose a portion of said lower electrode layer, *wherein a portion of the dielectric is removed from an intermediate region between the top electrode and the bottom electrode layer*;
>
> subsequently forming a conformal insulating layer over at least a portion of said exposed portion of the bottom electrode layer proximate to said exposed dielectric layer, said exposed dielectric layer and at least part of said top electrode layer proximate to said exposed dielectric layer, *whereby a portion of the conformal insulating layer is formed in said intermediate region*...,

where the portions with the added emphasis where added in the previous Amendment. Claims 4 and 36 contain similar language and have been similarly amended.

The present Office Action added these limitations to its previous rejection, stating that these are found in the primary reference, Takahashi, US patent number 5,683,931, referring to Figures 2C and 2D. This is respectfully submitted to be in error. Neither the figures nor the corresponding text of the specification (column 2, lines 19-27) teach, suggest or indicate either the that a portion of the capacitor dielectric is removed from the region intermediate to the electrodes or that a subsequent insulating layer fills this region back in. As can be seen from Takahashi's Figure 2C, the sides of the capacitor dielectric 305 are flush with the sides of the top electrode plate 306. There is no indication, suggestion, or teaching of the sort of undercutting into the intermediate region between the top electrode and the bottom electrode layer as indicated in Figure 3 of the present application at reference number 180. In

Figure 2D of Takahashi, the dielectric layer 307 is also shown to have a distinct boundary flush with the sides of the top plate 306 and not intruding into the intermediate region, as shown in Figure 4 of the present application.

The features of the independent claims 3, 4, and 36 that are emphasized above are neither taught, suggested, nor indicated by Takahashi or any other of the cited references. Consequently, there is no supporting evidence provided in the Office Action for the rejection of claims 3-11, 36-39, and 72-74, all of which contain this or a similar limitation. It is respectfully submitted that these rejections do not make the necessary *prima facie* case of obviousness, and that, on that basis, the rejection of claims 3-11, 36-39, and 72-74 must be withdrawn.

In its Response to Arguments portion, the Office Action states "In response to the applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which the applicant relies (i.e., 'inter-plate undercutting') are not recited in the rejected claims(s)." This also respectfully submitted to be in error. As quoted above (where the emphasis is again added), these claims contain the language "*wherein a portion of the dielectric is removed from an intermediate region between the top electrode and the bottom electrode layer*". This is believed to be a clear and concise representation of the inter-plate undercutting and it is unclear on what basis the Office Action has determined that this feature is missing from the claims.

The Office Action additionally rejected claim 78 and its dependent claim 79 under 35 U.S.C. 112, second paragraph. Accordingly, claim 78 has been amended to make its language clearer and is not believed to be indefinite as currently written.

Claims 26-30 and 78-80 are drawn to another exemplary embodiment of the formation of a capacitor in a CMOS process flow including an anti-reflective layer. The Office Action rejected these claims under 35 U.S.C. 103(a) with Kayanuma *et al.*, U.S. patent number 5,397,729 as the primary reference. Claim 26 is an independent claim, with claims 27-30 and 78-80 being dependent upon it. Claim 26 contains the limitation:

> ...removing a portion of said top electrode layer to expose a portion of the dielectric layer *thereby forming a top electrode, wherein the bottom electrode layer is not exposed*...

where the emphasis is added. The Office Action refers to Figures 4D and 4E of Kayanuma *et al.*: however, Figure 4D of Kayanuma *et al.* clearly shows that the bottom electrode 52 is exposed when the top electrode 54 is formed. On either side of the oxide layer 57, the bottom electrode layer 52 is clearly exposed when layers 53 and 57 are removed using resist 58 when going from Figure 4C to Figure 4D. Although the lower electrode is later covered by layer 59 in Figure 4E, it is exposed as part of the step forming the top electrode. Consequently, the primary reference of Kayanuma *et al.* clearly teaches away from the process of "removing a portion of said top electrode layer to expose a portion of the dielectric layer thereby forming a top electrode, wherein the bottom electrode layer is not exposed". Consequently, these rejections do not make the necessary *prima facie* case of obviousness and the rejection of claims 26-30 and 78-80 under 35 U.S.C. 103(a) with Kayanuma *et al.* as the primary reference is not believed to be well founded and should be withdrawn.

Conclusion

For any of these reasons, reconsideration of the Office Action's rejection of claims 3-11, 26-30, 36-39, 72-74, and 78-85 and consideration of new claims 86-101, is therefore respectfully requested, and an early indication of their allowability is earnestly solicited.

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Respectfully submitted,

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Date

APPENDIX

Pending Claims

(Claims 1 and 2 have been cancelled.)

3.(Previously Amended) A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer, thereby forming a top electrode;

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subsequently removing at least a portion of said exposed portion of the dielectric layer to expose a portion of said lower electrode layer, wherein a portion of the dielectric is removed from an intermediate region between the top electrode and the bottom electrode layer;

subsequently forming a conformal insulating layer over at least a portion of said exposed portion of the bottom electrode layer proximate to said exposed dielectric layer, said exposed dielectric layer and at least part of said top electrode layer proximate to said exposed dielectric layer, whereby a portion of the conformal insulating layer is formed in said intermediate region; and

forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of the conformal insulating layer.

4.(Previously Amended) A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer, thereby forming a top electrode;

subsequently removing at least a portion of said exposed portion of the dielectric layer to expose a portion of said lower electrode layer, wherein a portion of the

dielectric is removed from an intermediate region between the top electrode and the bottom electrode layer;

subsequently forming a conformal insulating layer over at least a portion of said exposed portion of the bottom electrode layer proximate to said exposed dielectric layer, said exposed dielectric layer and at least part of said top electrode layer proximate to said exposed dielectric layer, whereby a portion of the conformal insulating layer is formed in said intermediate region; and

forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of conformal insulating layer, wherein said conformal insulating layer has a thickness in the range of from 20Å to 70Å.

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5. The method according to claim 4, wherein said conformal insulating layer is an oxide layer is formed in a thermal process.

6. The method according to claim 5, wherein said thermal process is a rapid thermal oxidation is performed for a length of time in the range of from 10 to 60 seconds and at a temperature in the range of from 850°C to 1050°C.

7. The method according to claim 4, wherein said conformal insulating layer is formed by deposition.

8. The method of claim 3, wherein said ARL is an anti-reflective coating.

9. The method of claim 3, wherein said ARL is titanium nitride.

10. The method of claim 3, wherein said ARL is a plasma enhanced chemical vapor deposition anti-reflective layer (PEARL).

11. The method according to claim 10, wherein the plasma enhanced chemical vapor deposition anti-reflective layer has a thickness in the range of from 300Å to 400Å.

(Claims 12-25 have been cancelled)

26.(Previously Amended) A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer thereby forming a top electrode, wherein the bottom electrode layer is not exposed;

forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of said top electrode and said exposed portion of the dielectric layer; and

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subsequently removing a portion of said exposed portion of the dielectric layer and a portion of said bottom electrode layer, thereby exposing at least a portion of said semiconductor body and forming one or more capacitors.

27. The method according to claim 26, wherein said ARL is an anti-reflective coating.

28. The method according to claim 26, wherein said ARL is titanium nitride.

29. The method according to claim 26, wherein said ARL is a plasma enhanced chemical vapor deposition anti-reflective layer (PEARL).

30. The method according to claim 26, wherein said bottom electrode layer is additionally used to form the gate of one or more transistors formed on said integrated circuit.

(Claims 31-35 have been cancelled.)

36.(Previously Amended) A method of forming an integrated circuit comprising:

forming a conductive layer on a semiconductor body;

forming a capacitor structure, comprising:

a top electrode over a portion of said conductive layer; and

a dielectric layer between said top electrode and said conductive layer;

forming a conformal insulating layer over said capacitor structure and at least a portion of said conductive layer proximate to capacitor structure, whereby a portion of said conformal layer is formed in the region between the top electrode and the conductive layer;

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forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of the conformal layer;

forming a patterned mask over the ARL; and

etching said conductive layer using said patterned mask.

37. The method according to claim 36, wherein said conformal insulating layer has a thickness in the range of from 20Å to 70Å.

38. The method according to claim 37, wherein said conformal insulating layer is an oxide layer is formed in a thermal process.

39. The method according to claim 36, wherein said conductive layer is additionally used to form the gate of one or more transistors formed on said integrated circuit.

(Claims 40-71 have been cancelled)

72. The method of claim 3, further comprising:

forming a photoresist over at least a portion of the anti-reflective layer; and

irradiating said photoresist, wherein the anti-reflective layer reduces the reflectivity to the radiation that penetrates said photoresist by 70% or more.

20

73. The method of claim 72, wherein the anti-reflective layer reduces the reflectivity to the radiation that penetrates said photoresist by 70% to 85%.

74. The method of claim 3, wherein said anti-reflective layer is a Si_xON_y film.

(Claims 75-77 have been cancelled)

78.(Currently Amended) The method of claim 26, further comprising:

forming a photoresist over at least a portion of said anti-reflective layer;

irradiating said photoresist, wherein the anti-reflective layer reduces the reflectivity to the radiation that penetrates said photoresist by 70% or more; and

wherein said subsequently removing a portion of said exposed portion of the dielectric layer and a portion of said bottom electrode layer comprises performing an etch using said photoresist.

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79. The method according to claim 78, wherein the anti-reflective layer reduces the reflectivity to the radiation that penetrates said photoresist by 70% to 85%.

80. The method according to claim 26, wherein said anti-reflective layer is a Si_xON_y film.

81.(Currently Amended) A method of forming an integrated circuit, comprising:

a process flow for forming one or more transistors including:

forming a conductive layer on a semiconductor body;

subsequently forming an anti-reflective layer; and

defining and etching the conductive layer using the anti-reflective layer; and

performing a capacitor process module subsequent to said forming a conductive layer and prior to said forming an anti-reflective layer, comprising:

forming a top capacitor electrode over a portion of said conductive layer; and

forming a capacitor dielectric between said top electrode and said conductive layer, wherein said defining and etching the conductive layer forms the gate of one or more transistors and a bottom capacitor electrode,

wherein the process parameters of the portions of said process flow for forming one or more transistors prior to and subsequent to said performing a capacitor process module are optimized with the capacitor process module omitted, and wherein the process parameters for the capacitor module are optimized for capacitor formation while maintaining the process parameters of said process flow for forming one or more transistors optimized with the capacitor process module omitted.

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82.(Currently Amended) The method of claim 81, wherein said forming a top capacitor electrode and said forming a capacitor dielectric comprises:

forming a dielectric layer over at least a portion said conductive layer;

forming a top electrode layer over at least a portion of said conductive layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer, thereby forming said top capacitor electrode; and

removing at least a portion of said exposed portion of the dielectric layer to expose a portion of said conductive layer, thereby forming said capacitor dielectric between said top electrode and said conductive layer; and

wherein said capacitor process module further comprises:

forming a conformal insulating layer over the structure resultant from said removing at least a portion of said exposed portion of the dielectric layer.

83.(Currently Amended) The method of claim 82, wherein the thickness of said conformal insulating layer is selected to optimize the capacitor formation while maintaining the process parameters of said process flow for forming one or more transistors optimized with the capacitor process module omitted.

84. The method of claim 82, wherein said conformal insulating layer has a thickness in the range of from 20Å to 70Å.

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85.(Currently Amended) The method of claim 81, wherein said defining and etching the conductive layer using the anti-reflective layer comprises:

forming the anti-reflective layer over the conductive layer, the top capacitor electrode and the dielectric layer between said top electrode and said conductive layer;

forming a patterned mask over the anti-reflective layer; and

etching said conductive layer using said patterned mask.

86.(New) A method, comprising:

a) defining a CMOS process flow, comprising:

i) optimizing parameter values of a transistor flow to form a conductive layer, thereafter to form an anti-reflective layer on the conductive layer, and thereafter to define and etch the conductive layer using the anti-reflective layer, whereby the control gates of one or more transistor gates are formed, and wherein said etch is performed using a photoresist and said parameter values of the transistor flow include the thickness of the photoresist; and

ii) subsequently defining parameter values for a capacitor module to form a capacitor structure comprising a top electrode over a portion of said conductive layer and a capacitor dielectric therebetween and thereafter to form an insulating structure, wherein said defining and etching the conductive layer using the anti-reflective layer additionally forms a bottom electrode for said capacitor structure, and wherein the parameter values for the insulating structure of the capacitor module are optimized to electrically isolate the top electrode from the bottom electrode without changing the previously optimized parameter values of said transistor flow; and

b) forming an integrated circuit including one or more capacitors according to said CMOS process flow.

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87.(New) The method of claim 86, wherein said insulating structure includes:

a conformal dielectric layer formed over said capacitor structure, wherein said parameter values for the insulating structure of the capacitor module includes a thickness for said conformal dielectric layer.

88.(New) The method of claim 86, wherein said CMOS process flow is for a process on a scale of 0.35μm or less

89.(New) The method of claim 86, wherein the said parameter values of the transistor flow further include thickness of said antireflective layer.

90.(New) The method of claim 86, wherein said capacitors have a leakage current of not greater than $4fA/\mu m^2$.

91.(New) A method of forming an integrated circuit, comprising, in a first sector and a second sector, a process of:

a) forming a conductive layer on a semiconductor body;

b) forming an anti-reflective layer over the conductive layer;

c) forming a patterned mask over the anti-reflective layer; and

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d) etching the conductive layer using the patterned mask, thereby forming the gate of one or more transistors in the first sector, wherein a), b), c) and d) are performed according to a first set of process parameters including the thickness of said mask that have been optimized for said gate formation; and

the method further comprising, in said second sector, performing a process prior to said forming an anti-reflective layer comprising:

e) forming a capacitor structure including a top electrode over a portion of said conductive layer and a capacitor dielectric therebetween, wherein said etching additionally forms a bottom capacitor electrode in the second sector; and

f) forming an insulating structure over the capacitor structure, wherein said forming an insulating structure is performed according to a second set of process parameters optimized to electrically isolate said top electrode from the conductive layer while keeping said first set of process parameters the same.

92.(New) The method of claim 91, wherein said forming an insulating structure comprises:

forming a conformal dielectric layer over said capacitor structure and said conductive layer, wherein the second set of process parameters includes a thickness for said conformal dielectric layer.

93.(New) The method of claim 91, wherein the method is for a CMOS fabrication process.

94.(New) The method of claim 93, wherein the method is for a CMOS processes on a scale of $0.35\mu m$ or less.

95.(New) The method of claim 91, wherein the first set of process parameters further includes the thickness of said antireflective layer.

96.(New) The method of claim 91, wherein the method forms a capacitor structure having leakage current between the top electrode from the conductive layer of not greater than $4fA/\mu m^2$.

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97.(New) A CMOS fabrication method, comprising:

a) performing a first fabrication process on a first semiconductor body, comprising:

forming a conducting layer on the first semiconductor body;

forming an antireflective layer over the conductive layer;

forming a patterned photoresist layer over the antireflective layer; and

etching the conductive layer using said patterned photoresist layer into gates for one or more transistors, wherein said forming a conducting layer, forming an antireflective layer, forming a patterned photoresist layer, and etching the conductive layer in the first fabrication process on the first semiconductor body are defined by a first set of process parameters including the thickness of said photoresist that are optimized for said gate formation; and

b) performing a second fabrication process on a second semiconductor body, comprising:

forming a second conducting layer on the second semiconductor body;

forming a capacitor structure including a top electrode over a portion of the second conductive layer and an inter-electrode therebetween;

forming an antireflective layer over the second conductive layer and the capacitor structure;

forming a patterned photoresist layer over the second antireflective layer;

etching the conductive layer using said patterned photoresist layer, thereby forming a lower capacitor electrode for the capacitor structure, wherein said forming a

conducting layer, forming a antireflective layer, forming a patterned photoresist layer, and etching the conductive layer in the second fabrication process on the second semiconductor body are defined by said first set of process parameters; and

forming, subsequent to said forming a capacitor structure and prior to said forming a antireflective layer, an insulating structure defined by a second set of process parameters optimized for electrically isolating the top electrode from the conductive layer while keeping first set of process parameters the same.

98.(New) The method of claim 97, wherein said forming an insulating structure comprises:

forming a conformal dielectric layer formed over said capacitor structure and said conductive layer, wherein the second set of process parameters includes a thickness for said conformal dielectric layer.

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99.(New) The method of claim 97, wherein said first and second fabrication processes are for CMOS processes on a scale of 0.35μm or less.

100.(New) The method of claim 97, wherein the first set of process parameters further includes the thickness of said antireflective layer.

101.(New) The method of claim 97, wherein the second fabrication process forms a capacitor structure having leakage current between the top electrode from the conductive layer of not greater than 4fA/μm^2.